https://doi.org/10.36375/prepare_u.iei.a189

# 21 Level Asymmetric Inverter without Inversion Circuit with Reduced Switch Count

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***Abstract*—This paper gives a new design for asymmetrical Multi-Level Inverter without H-bridge and with reduced number of switch components. The proposed model produces 21 levels with only 10 switches and 3 unequal voltages to obtain a maximum voltage output. The modes of operation of the proposed circuit are discussed in detail in this paper and there by framing the switching sequence for the proposed circuit. Simulation of the proposed inverter is done for loads like Resistive and Reactive. From the simulation results, inverter performance is analyzed in terms of THD.**

***Keywords—Power electronics, Asymmetric inverter, reduced switch component, modes of operation,***

## I. INTRODUCTION

Multi-Level Inverters (MLI) have become a revolution in the world of power electronics for its improved voltage and current waveforms, high power applications and for power quality demanding applications. They also find applications in Speed drive control, STATCOMS, HVDC and HVAC transmissions. The advantages of multi-level inverters are higher voltage operating capability, reduced voltage derivatives, voltages with reduced harmonic components, fault tolerant operation and increased efficiency. The current trend applications for multi-level inverters are around photovoltaic conversions, electric vehicle technology, wind energy technology etc. Multi-level inverter is made up of switches, diodes, and voltage sources. Based on the construction of the circuit and the voltage sources considered it can be classified as symmetric and asymmetric MLIs and to be specific they are further classified as neutral point clamped (NPC), flying capacitor (FC) and cascaded H-Bridge (CHB) [1]-[2]. All these types of conventional type MLIs have a greater number of switches in their design that is the main reason in going for inverters with many topologies and structures that will reduce the switching components of the circuit.

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The required parameters for the design of a MLI are number of levels to be acquired, number of switches needed for the required levels, the THD of the output voltage, the number of independent DC sources needed to generate the required levels, switch stress and the total standing voltage (TSV).

However, for the increased number of levels, a greater number of switches are required to achieve the higher levels. So, a solution is needed to have a greater number of levels and have a reduced number of switching components [3]-[6].

Considering the above, many attempts are being made in the past few years to reduce the switch count and those works are discussed in [7]-[11]. These works have given some new structures and topologies with reduced count but having its own shortcomings. The proposed model is also a new topology structure with reduced switching component and taken into consideration of the shortcomings to produce a much higher level of output. The proposed model is a new topology for 21-level asymmetric MLI with only 10 switches and 3 unequal DC sources.

This paper follows through as given in Section II gives the model of the proposed circuit following by Section III which provides the working, modes of operation and the switching sequence of the proposed circuit in a detail manner. Section IV is the simulation and results of the proposed model. Finally in Section V conclusions are being made in how the

proposed model gives a higher voltage with reduced switch count and reduced THD.

## II. 21-LEVEL INVERTER WITH SWITCHING SEQUENCE

A MLI topology [12] with reduced switch count is shown in figure 1. To obtain 21 levels, the proposed circuit consists of 10 switches and 3 voltage sources. Here all 10 switches are unidirectional in nature as shown in figure 2, so that similar driver circuit can be used for all the switches present in the circuit. A basic sinusoidal PWM technique is used for the switching operation to give the triggering for the proposed model. The designed MLI circuit is formed with 3 unequal voltage sources which will make an asymmetric configuration of those voltage sources that are selected as 40V, 80V and 280V respectively.

### *A. MLI Design Criteria*

For the inverter topology, mathematical equation is derived in order to find the number of levels obtained from the inverter and number of switches and number of voltage sources required for the inverter. Let the number of voltage sources be *m*, number of switches be $N_{sw}$, number of levels of the inverter be $N_{lvl}$.

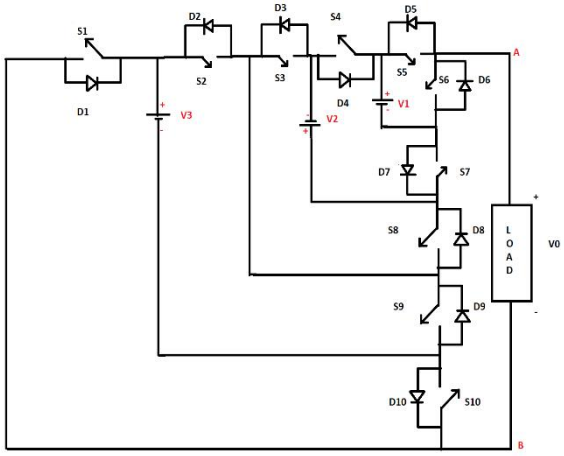


Fig 1. 21 Level Inverter [12]

Fig 2. Switch Configuration

The number of switches for the proposed inverter can be calculated as,

$$N_{sw} = 2^m + 2 \quad \text{- - - - - - - - - - (1)}$$

The number of levels for the proposed inverter can be calculated as,

$$N_{lvl} = 7 \times m \quad \text{- - - - - - - - - - (2)}$$

The peak output voltage of the inverter can be calculated as follows,

$$V_{0,\,max} = (2^m + 2) \times V_{DC} \quad \text{- - - - - - - - - (3)}$$

Now the proposed topology consists of 3 voltage sources (*m = 3*), so the number of switches $N_{sw}$ = 10, the number of levels of the inverter is $N_{lvl} = 21$. Here the $V_{DC} = V_1 = 40V$, so the peak output voltage can be given as $V_{0,\,max} = 400V$.

## III. MODES OF OPERATION

The inverter is designed to work in 21 modes of operation to construct an alternating waveform. For understanding purpose, few modes are explained in fig 3. Device status for each mode of operation is given below,

Mode-1: $S_2$, $S_3$, $S_5$, $S_7$, $S_{10}$ devices are ‘ON’ to generate 400V

Mode-2: $S_2$, $S_3$, $S_6$, $S_7$, $S_{10}$ devices are ‘ON’ to generate 360V

Mode-3: $S_2$, $S_5$, $S_7$, $S_8$, $S_{10}$ devices are ‘ON’ to generate 320V

Mode-4: $S_2$, $S_3$, $S_4$, $S_5$, $S_{10}$ devices are ‘ON’ to generate 280V

Mode-5: $S_2$, $S_3$, $S_4$, $S_6$, $S_{10}$ devices are ‘ON’ to generate 240V

Mode-6: $S_1$, $S_3$, $S_6$, $S_7$, $S_9$ devices are ‘ON’ to generate 200V

Mode-7: $S_2$, $S_4$, $S_6$, $S_8$, $S_{10}$ devices are ‘ON’ to generate 160V

Mode-8: $S_3$, $S_5$, $S_7$, $S_9$, $S_{10}$ devices are ‘ON’ to generate 120V

Mode-9: $S_9$, $S_6$, $S_7$, $S_9$, $S_{10}$ devices are ‘ON’ to generate 80V

Mode-10: $S_5$, $S_7$, $S_8$, $S_9$, $S_{10}$ devices are ‘ON’ to generate 40V

Mode-11: $S_6$, $S_7$, $S_8$, $S_9$, $S_{10}$ devices are ‘ON’ to generate 0V

Mode-12: $S_3$, $S_4$, $S_6$, $S_9$, $S_{10}$ devices are ‘ON’ to generate -40V

Mode-13: $S_4$, $S_5$, $S_8$, $S_9$, $S_{10}$ devices are ‘ON’ to generate -80V

Mode-14: $S_4$, $S_6$, $S_8$, $S_9$, $S_{10}$ devices are ‘ON’ to generate -120V

Mode-15: $S_1$, $S_3$, $S_5$, $S_7$, $S_9$ devices are ‘ON’ to generate -160V

Mode-16: $S_1$, $S_3$, $S_6$, $S_7$, $S_9$ devices are 'ON' to generate -200V

Mode-17: $S_1$, $S_5$, $S_7$, $S_8$, $S_9$ devices are 'ON' to generate -240V

Mode-18: $S_1$, $S_6$, $S_7$, $S_8$, $S_9$ devices are 'ON' to generate -280V

Mode-19: $S_1$, $S_3$, $S_4$, $S_6$, $S_9$ devices are 'ON' to generate -320V

Mode-20: $S_1$, $S_4$, $S_5$, $S_8$, $S_9$ devices are 'ON' to generate -360V

Mode-21: $S_1$, $S_4$, $S_6$, $S_8$, $S_9$ devices are 'ON' to generate -400V

From the modes of operation, switching sequence for the positive and negative levels of the inverter can be framed and it is shown in Table 1.

Table 1: Switching Sequence

| Mode | Levels | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | $S_7$ | $S_8$ | $S_9$ | $S_{10}$ | $V_o$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 10 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | +40 V |
| 2 | 9 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | +36 V |
| 3 | 8 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | +32 V |
| 4 | 7 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | +28 V |
| 5 | 6 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | +24 V |
| 6 | 5 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | +20 V |
| 7 | 4 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | +16 V |
| 8 | 3 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | +12 V |
| 9 | 2 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | +80 |
| 10 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | +40 |
| 11 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0V |
| 12 | -1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | -40 |
| 13 | -2 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | -80 |
| 14 | -3 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | -120 |
| 15 | -4 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | -160 |
| 16 | -5 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | -200 |
| 17 | -6 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | -240 |
| 18 | -7 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | -280 |
| 19 | -8 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | -320 |
| 20 | -9 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | -360 |
| 21 | -10 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | -400 |

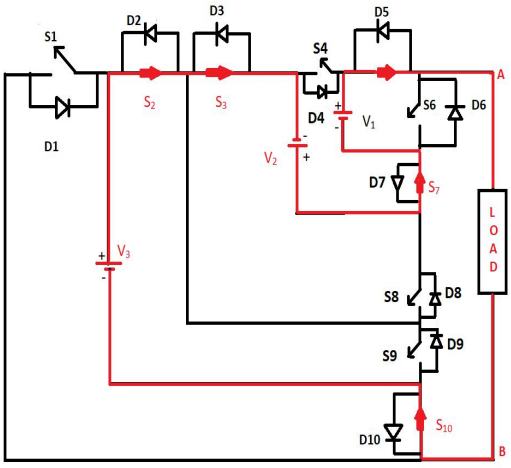


**Fig 3(a) Mode-1 (+400V)**

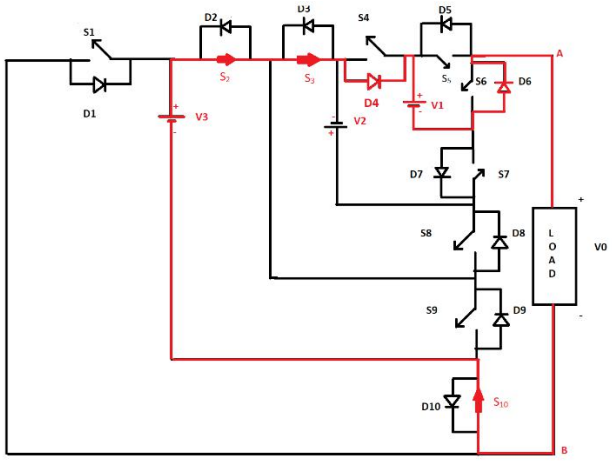


**Fig 3 (b) Mode-5 (+240V)**

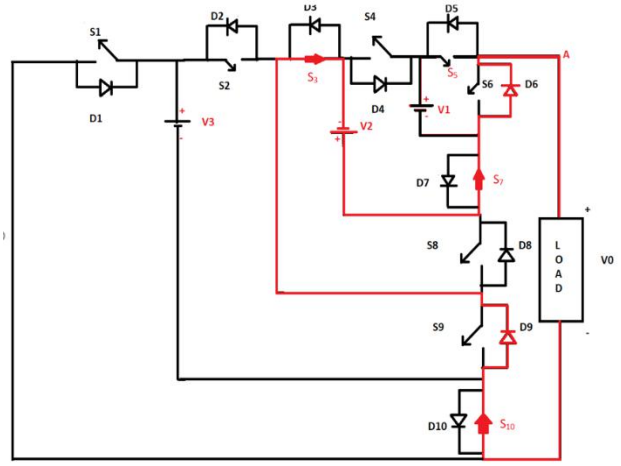


**Fig 3 (c) Mode-9 (+80V)**

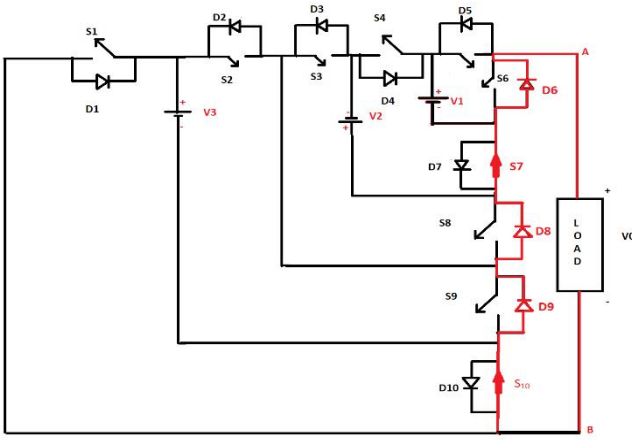


**Fig 3 (d) Mode-11 (0V)**

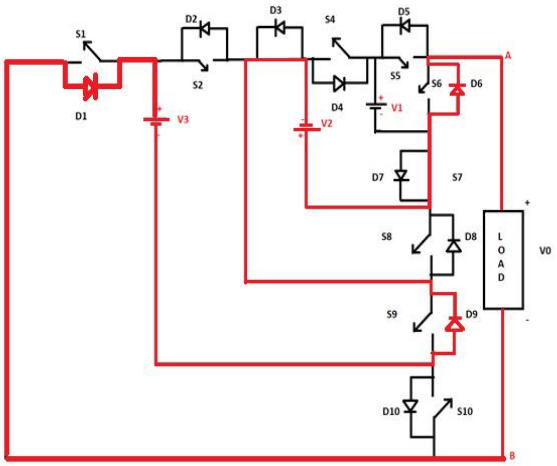


**Fig 3 (e) Mode-16 (-200V)**

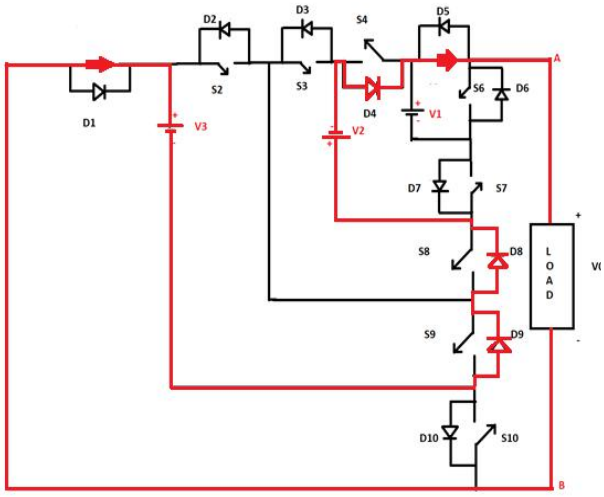


**Fig 3 (f) Mode-20 (-360V)**

**Fig 3 Modes of Operation for 21 level inverter**

## IV. Simulation and Results

The proposed inverter is simulated in MATLAB/SIMULINK with resistive load of 150 Ω and the simulated result is shown in fig 4. THD of the inverter's output voltage is 4.73% which is well within the range of IEEE Recommended Practices and Requirements for Harmonic Control in Electric Power Systems (IEEE 519). The proposed circuit produces a peak-to-peak voltage of ±400V as shown in fig 4.

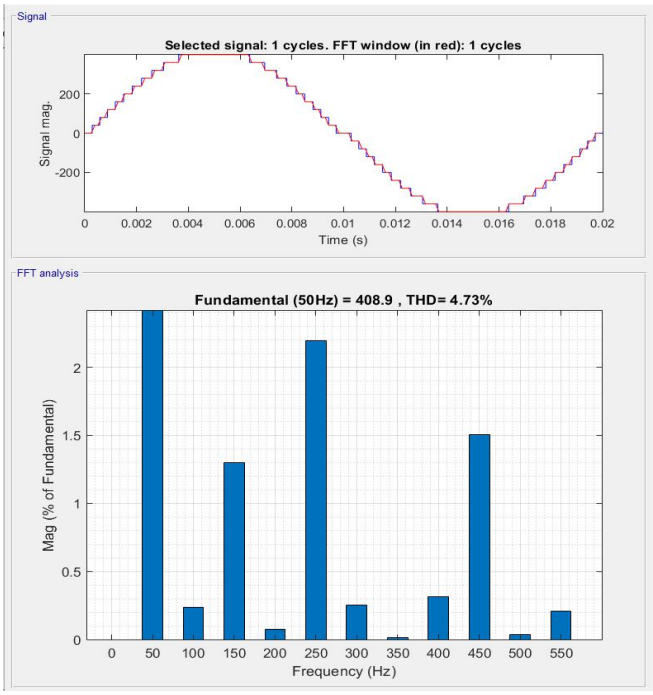


Fig 4.Simulation result of 21-level inverter for R-load

Furthur, the proposed circuit is simulated for a R-L load, with R=150 Ω, L = 0.477H. The output voltage for the R-L load for the proposed inverter is as shown in fig 5 and the THD for the proposed inverter's output voltage is 4.82%.

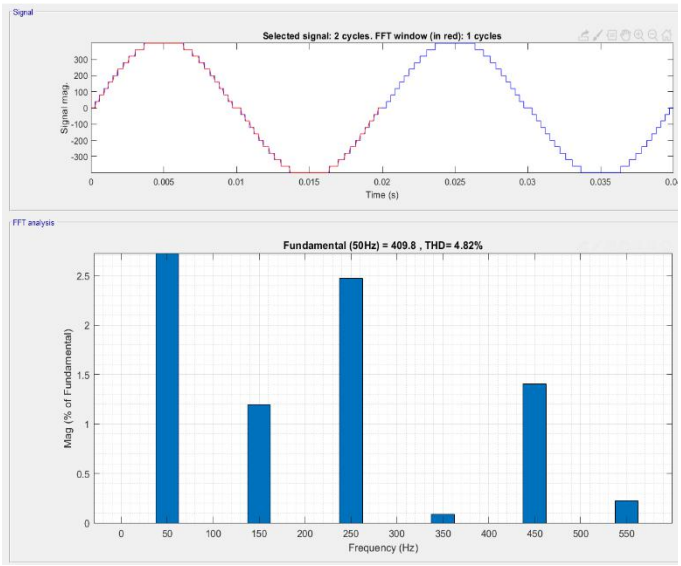


Fig 5.Simulation of 21-level inverter with R-L Load

## V. CONCLUSION

A new topology with 21 level multi-level inverter with reduced switch count has been discussed in detail in this paper. The proposed circuit can achieve the maximum voltage with minimum number of switches with a low THD, thereby reducing the cost and size. Comparison between the proposed circuit, neutral point clamped MLI (NPC), flying capacitor MLI (FC) and cascaded H Bridge (CHB) circuit are shown in from Fig 5 (a) to Fig 5 (c).

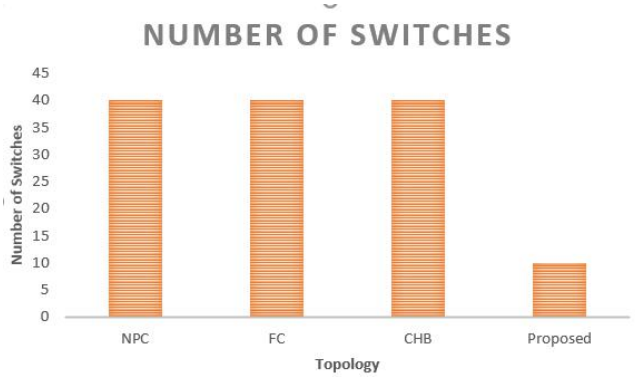


Fig 5(a)

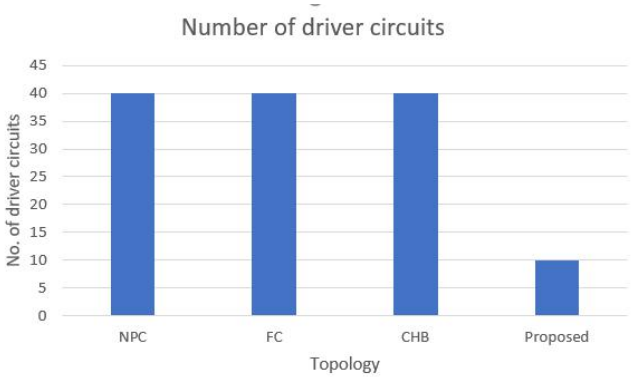


Fig 5(b)

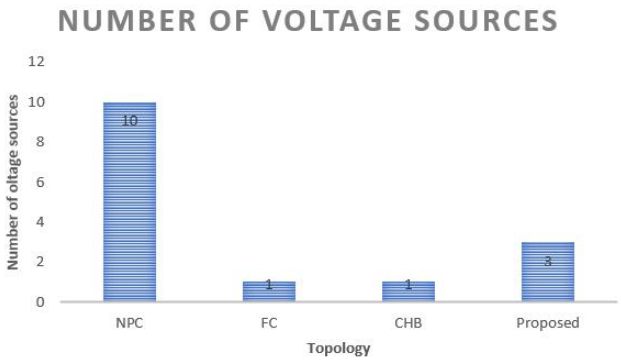


Fig 5(c)

## ACKNOWLEDGEMENT

The authors thank the Department of Electrical and Electronics Engineering, Anna University, India for the financial support through RUSA 2.0 (PO 2) project

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