https://doi.org/10.36375/prepare_u.iei.a200

Design, Simulation and Analysis of A Novel EBG Structure using Advanced Design System: Implementation and Related Issues

Y.Uma Maheswari
MIE, Research Scholar, EEE
Karpagam Academy of Higher Education, Coimbatore-641021
yummyaskisan@gmail.com

Dr.A.Amudha
Professor and Head, EEE
Karpagam Academy of Higher Education, Coimbatore-641021
amudha.a@kahedu.edu.in

Dr.L.Ashok Kumar
FIE, C.Engr (IE), Professor, Dept of EEE
P.S.G.College of Technology, Coimbatore-641004
askipsg@gmail.com

Corresponding author's email: yummyaskisan@gmail.com

Abstract - Electromagnetic noise is a operational disturbances in the high frequency operational circuits. Parasitic filters are not efficient in the case of high frequency electronic circuits. In order to mitigate the noise level in such circuits, novel electromagnetic bandgap structure is designed, simulated and measured the noise level. Electronic design automation (EDA) tools help for these work and provide the designer to prevent the rework which leads to time and cost savings. It is essential to understand the capabilities of the tool. This paper gives the design and simulation procedure of the Novel L Bridge with double square embedded Electromagnetic Bandgap structure (EBG) for the frequency range 0 GHz to 10 GHz and the same structure is implemented in hardware and measured the results using R&S®ZVH Vector Network Analyzer. It is observed that the simulated and measured results are in good alignment with the result values.

Key words: EMI; EM Simulation tools; printed circuit board (PCB)

INTRODUCTION

As the operational frequency of the digital circuit increases, there exist the simultaneous switching noises, electromagnetic interference which creates the unwanted effects in the circuit as well as to the proximity devices. Transmission of the noise can be in two ways, either it could be conduction medium or it can be radiated medium. Introducing the parasitic filters is not very effective in the case of high frequency operations [1-4]. Various methods can be adopted in the design stage, at the software levels and hardware levels. It is essential to mitigate those noises at the source level and in the conduction path.

The power supply module, power electronic components, component packaging, improper printed circuit board layout method, external disturbances, near-by channel interferences, and other elements in the devices may all play a role in the problem. Radiated and conducted energy may both be emitted from a same device [5-6]. The unwanted signal that gets mixed up with the intended signal. Interference occurs when noise affects a circuit in an unanticipated manner. Taking care of this issue at the source level is essential. Electromagmetic compatibility (EMC) is primarily determined by the PCB design layout and guidelines in the vast majority of electronic items [7-8]. PCB design layout and standards have a significant influence on electromagnetic interference (EMI). An electromagnetic environment (EMC) is a kind of electromagnetic interference that affects the reliability of any electronic device.

In the case of high frequency in terms of several GHz, Electromagnetic Band gap (EBG) structure helps to mitigate the noise in the transmission path which acts as a filter. This paper focuses on the EBG filter for mitigating the conductive noise in the circuit [9-16].

This paper covers the following topics:

- Introduction to EDA tool
- EBG structure
- ADS design capabilities
- Design and Simulation procedure of EBG structure
- Hardware
- Results and Discussion.

INTRODUCTION TO EDA TOOL

https://doi.org/10.36375/prepare_u.iei.a200

Electronic design automation tool are very essential for designing electronic circuits, IC design, Printed circuit board design and other design work related to electronics. These tools help the designer to check the functionality prior to prototyping, avoiding rework and reduces the cost and time. Each activity had the definite design flow to accomplish the work [17 – 20].

EDA tool development encountered various stages. Initially it was referred as CAD where the activities are carried out in two dimensions with their editor. Next is CAE, advancement from the previous stage where it was possible to synthesize, to optimise can be performed with less intelligence. Subsequent stage is EDA where it is possible to perform all the automation with rich intelligence.

Application of EDA tools such as MATLAB, PSPICE, etc,. are used in designing electronic circuits. EDA tools such as Altium Designer, OrCAD, Allegro etc are used for designing printed circuit board. EDA tools such as CST, EMPro, ADS, SIWave etc are used for simulating the signal and power for their integrity and to simulate the conducted and radiated emission if the circuit. EDA tool such as Xilinx used to design the FPGA, ASIC related packages. In the field of embedded design, with the help of these advanced EDA tools it is possible to integrate hardware logic with independent IP rights, System On Chip, hardware and software co design [18-22].

EDA tools have various editors such as graphical editor, text editor, wave form editor to perform specific functionalities. Simulation tools for knowing the signal and power characteristics, electromagnetic characteristics and thermal properties of the design. Analysis tool for examining the design logic and electrical characteristics. Synthesis tool is used for the conversion of the hardware description languages and optimization of the logic levels in the data path [23-25].

In this paper, Electromagnetic Bandgap structure is designed; simulated using ADS tool and gerber file is generated for manufacturing using PCB technology.

EBG Structure

Electromagnetic Bandgap structure is regularly pattered symmetrical structure which acts as filter in case of high frequency operational electronic circuits (in GHz). The shape and pattern can be designed based on the band width requirements of the circuit. Based on the lower and upper cut off frequency, the structure can be designed. This structure has the advantage such that this can be integrated to the power or ground layers of printed circuit board. There are various types of EBGs based on the bandwidth requirement and the application which single band, dual band and multi band. Based on the implementation technology, EBG can be broadly of planar and mushroom types [23-30]. Due to the fabrication advantages, this paper discusses on the planar type EBG structure.

ADS Capabilities

Advanced Design System is an electronic design automation tool used which has various design features for designing and analysing high speed PCB circuits. It has two editors circuit and layout editors. Using the circuit editor, it is possible to create component, insert component with its corresponding models, can make connection between the components and to simulate the circuit. It is possible to create sub network and can be used in the main circuit. There are default libraries are also available in the library.

S-Parameter can be performed in the frequency domain by selecting the s-parameter simulation controller. In this mode, it is possible to input the frequency range. With the required frequency details, it is also possible to calculate the Y-Parameter, Z-Parameter and group delay. Any warnings or error can be noticed in the status window. Variety of plots can be plotted in data display. As in excel sheet, the results can be displayed in a different sheet with appropriate name, data display window which can be saved or printed.

Tuning can be used to change the parameter values of components in the circuit, based on the simulation results. By moving the slider in the turning dialog box, the result gets reflected dynamically in the graph based on the changes in the component values, thereby behaviour of the circuit is changing. The slider can be moved up to our desired response. Each response can be stored to optimise the values. Optimization of the design parameters can be done by selecting the components, minimum and maximum values of and the result are seen in the optimization cockpit window. With the available response, reverse engineering is also possible for creating the equivalent circuit.

Layout editor has the various types of the technology templates used for creating the design either from the circuit schematic or

https://doi.org/10.36375/prepare_u.iei.a200

directly out of this editor. In the layout editor, pcb substrate definition, material definition, padstack and via definition and line type definition are possible. Also constraint manager allows to set the clearance and routing constraints such as width and via [21].

Design Procedure And Simulation

In this paper novel planar type L Bridge with double square embedded EBG structure is designed. The dimension of the unit cell 30 mm x 30 mm is created initially based on Fig 1. Peripheral of the unit cell is created as L bridge type and the double square fashion is embedded inside it with symmetrical to both axis which forms the capacitance and inductance effects [31].

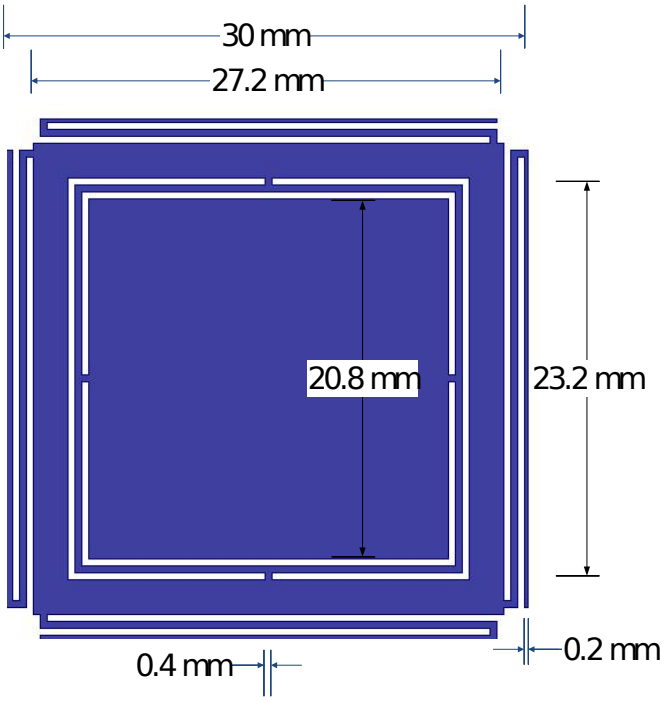

Fig.1 Unit cell with Dimension 30 mm x 30 mm

Unit cell is then arrayed to 3 x 3 matrix fashion with the entire dimension of the structure is 90 mm x 90 mm. In the EDA tool two ports are assigned to excite the signal. Port 1 is considered as input port and Port 2 is considered as receiver or measuring port. Fig 2 shows the capture of designed EBG structure.

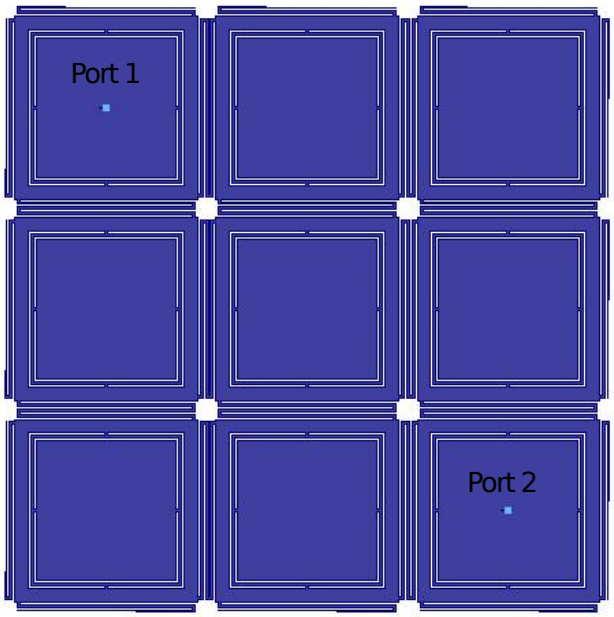

Fig.2 EBG Array with Dimension 90 mm x 90 mm

This EBG structure implemented in a PCB technology as shown in Fig 3. In this research, it is considered two PCB layers with layer 1 being EBG structure and layer 2 being continuous plane which can be ground or return plane [32-33]. PCB material taken here is FR4 with dielectric constant 4.6 and the dielectric thickness as 0.8 mm.

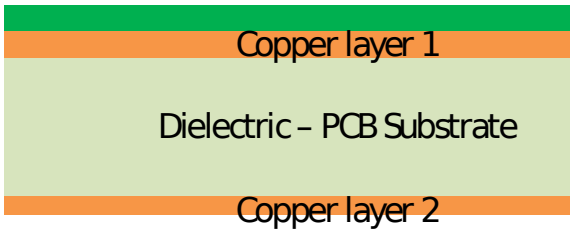

Fig.3 PCB stack up Cross section

Fig 4 shows the three dimensional view of the two layer substrate. For better understanding dielectric portion skipped and shown only copper area.

Once the structure design is completed, conducted noise is measured with the help of EM simulation. Before processing the simulation, it is necessary to set the type of EM simulator (momentum RF, momentum microwave or FEM), substrate details, port details, frequency plans etc. The simulation setting window is shown in Fig 5.

https://doi.org/10.36375/prepare_u.iei.a200

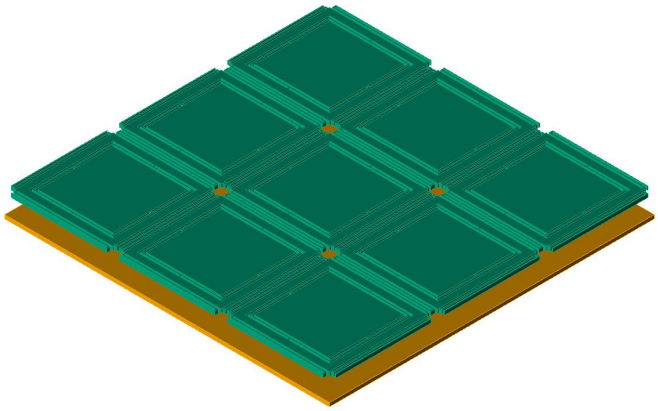

Fig. 4 3D view of EBG Array

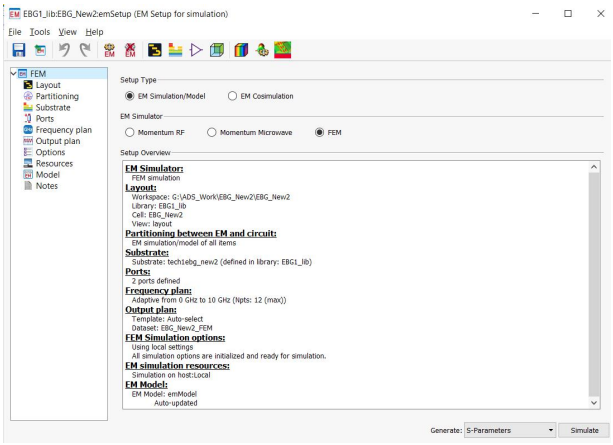

Fig. 5 EBG simulation setting

Upon completing the simulation setting, the design is ready to simulate. The simulation result shows the characteristic performance and noise depth can be measured from S-Parameter values. Simulation results of the EBG pattern is shown in the Fig 6. S_{11} and S_{22} give the reflection coefficient and S_{21} and S_{12} gives the transmission coefficient. With the help of these values, electromagnetic noise level can be measures. In this it is achieved 40 dB of noise depth over the frequency 1 GHz to 9 GHz.

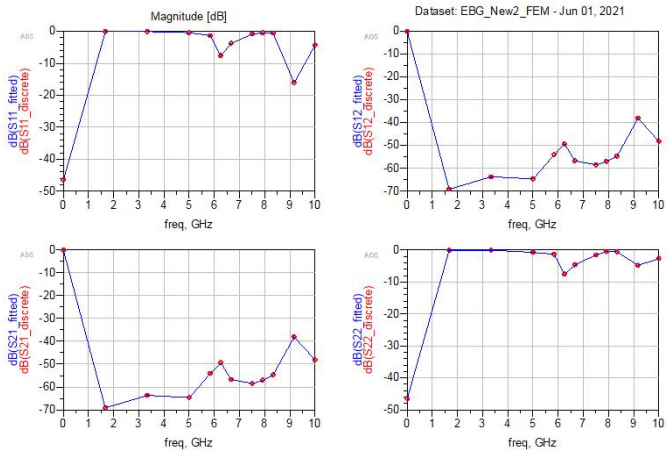

Fig. 6 Simulation results of the EBG pattern

HARDWARE MEASUREMENT

The hardware implementation of the designed EBG structure is being considered. In order to fabricate the structure, 274 X Gerber formats of the two-layers (EBG structure and the ground layer) is exported from the EDA tool, which is then provided to a fabricator for the purpose of manufacture a Printed Circuit Board (PCB). The Gerber format is a standardised file format that is generally acknowledged by the fabricator community. This file has the information on the shape and placement of the conductor. FR4 was selected as the board material due to the high quality and dependability of the material with the dielectric thickness as 0.08mm and the copper layer is 0.03mm.

R&S®ZVH Vector Network Analyzer is used to for measuring the conducted noise. SMA connectors are soldered on the fabricated PCB to excite and measure the signal. Here also the same frequency plan is set and probes of the instrument are connected to the SMA connectors so as to establish the connection. The hardware setup is shown as in the Fig 7. The S-Parameter results in terms of reflection and transmission coefficients are measured using the analyser.

https://doi.org/10.36375/prepare_u.iei.a200

Fig. 7 Hardware Measurement setup

Measurement result S_{11} is captured and shown in Fig 8 and S21 is captured and shown in Fig 9. The measured results are approximately matching with the simulated result. There can be seen slight variation that is due to the connector and cable connection.

Fig. 8 Measurement result – S11 parameter

Fig. 9 Measurement result – S21 parameter

Results and Discussion

In the simulation result shown in Fig 6, it is clearly seen that the noise level is -40 dB depth between the lower cut-off frequency 1 GHz and 9 GHz as upper cut-off frequency and for the noise level -38 dB depth between the lower cut-off frequency 1 GHz and 10 GHz as upper cut-off frequency with wider bandwidth from S_{21} parameter value. Maximum depth level -70 dB is achieved at 1.6 GHz.

In the hardware measurement result shown in Fig 9, it is absorbed at the -40 dB noise level 4 GHz to 7 GHz. This is approximately matching with the simulated result. The variations are due to cable and connector noise.

From the results, it is concluded that the introduction of the Electromagnetic bandgap structure in the PCB mitigates the noise upto the levels as mentioned in this section above. Depending upon the circuit product application and the frequency of the circuit operation, EBG structure can be selected and used to mitigate the conducted noise.

Conclusion

In this paper Novel L Bridge with double square embedded Electromagnetic Bandgap structure (EBG) is designed in order to mitigate the noise level in such circuits. The structure is simulated and measured for the conduction noise level. Electronic design automation (EDA) tool is used for simulation and R&S®ZVH Vector Network Analyzer is used to measure the conducted noise in PCB. The frequency sweep for simulation and hardware measurement is 0 to 10 GHz. From the simulated and hardware results, it is concluded that with the introduction of the Electromagnetic

bandgap structure in the PCB, mitigates the noise levels and it is observed that the simulated and measured results are in good alignment with the result values. Signal integrity issues can be extended in future work.

REFERENCES

[1]. J. Lau, C. Wong, J. Prince, and W. Nakayama, Electronic Packaging: Design, Materials, Process, and Reliability. New York: McGraw-Hill, 1998.

[2]. G.-T. Lei, R. W. Techentin, and B. K. Gilbert, “High-frequency characterization of power/ground-plane structures,” IEEE Trans. Microw. Theory Tech., vol. 47, pp. 562–569, May 1999.

[3]. S. Shahparnia and O. M. Ramahi, “Electromagnetic interference (EMI) reduction from printed circuit boards (PCB) using electromagnetic bandgap structures,” IEEE Trans. Electromagn.Compat., vol. 46, no. 4, pp. 580–587, Nov. 2004.

[4]. R. Abhari and G. V. Eleftheriades, “Suppression of the parallel-plate noise in high-speed circuits using a metallic electromagnetic band-gap structure,” in Proc. IEEE MTT-S Int. Microwave Symp., vol. 1, Jun. 2002, pp. 493–496.

[5]. T. Kamgaing and O. M. Ramahi, “A novel power plane with integrated simultaneous switching noise mitigation capability using high impedance surface,” IEEE Microw.Wireless Compon.Lette., vol. 13, no. 1, pp. 21–23, Jan. 2003.

[6]. R. Abhari and G. V. Eleftheriades, “Metallo-dielectric electromagnetic bandgap structures for suppression and isolation of the parallel-plate noise in high-speed circuits,” IEEE Trans. Microw. Theory Tech., vol. 51, no. 6, pp. 1629–1639, Jun. 2003.

[7]. S. Shahparnia and O. M. Ramahi, “Simultaneous switching noise mitigation in PCB using cascaded high-impedance surfaces,” Electron.Lett., vol. 40, no. 2, pp. 98–100, Jan. 2004.

[8]. Y Uma Maheswari, A Amudha, L Ashokkumar, Y Dhayaneswaran, “Study on Electro Magnetic Interference and Compatibility Across Various Levels and Mitigation Technique using Software”, Technical Volume of 35th Indian Engineering Congress, December, 2020

[9]. YahieaAlnaiemy1 , and Lajos Nagy 1 , 1 Budapest University of Technology and Economics, Budapest, Hungary, “Improved Antenna Gain and Efficiency Using Novel EBG Layer:, SoSE 2020 • IEEE 15th International Conference of System of Systems Engineering • June 2-4, 2020 Budapest, Hungary

[10]. R. Gonzalo, P. D. Maagt, and M. Sorolla, “Enhanced patch antenna performance by suppressing surface waves using photonic-band substrates,” IEEE Trans. Microwave Theory Tech., vol. 47, no.11, pp. 2123- 2130, Nov. 1999.

[11]. Li Yang; Mingyan Fan; Fanglu Chen; Jingzhao She; ZhengheFeng, “A novel compact electromagnetic-bandgap (EBG) structure and its applications for microwave circuits”, IEEE Transactions on Microwave Theory and Techniques Vol. 53, Issue: 1, Jan. 2005

[12]. Y. Ko, K. Ito, J. Kudo, and T. Sudo, “Electromagnetic radiation properties of a printed circuit board with a slot in the ground plane,” in Proc. Int. Symp. Electromagnetic Compatibility, Tokyo, Japan, May 17-21, 1999, pp. 576 - 579.

[13]. Yuan-Yuan Zhang, Wen-Sheng Zhao ✉ , Qi Liu and Gaofeng Wang, “Novel electromagnetic bandgap structure for wideband suppression of simultaneous switching noise”, Electronics Letters 14th November 2019 Vol. 55 No. 23 pp. 1243–1245

[14]. D. F. Sievenpiper, “High-impedance electromagnetic surfaces,” Ph.D. dissertation, Dept. Elect. Eng, Univ. California at Los Angeles, Los Angeles, CA, 1999.

[15]. Bruce Archambeault,Sam Connor ,“Review of Printed-Circuit-Board Level EMI/EMC Issues and Tools”, IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY, VOL. 52, NO. 2, MAY 2010

[16]. Y. Uma Maheswari, A. Amudha, L. Ashok Kumar, K. Nagasaravanan, Mohana Sundaram, Y. Dhayaneswaran, “Simulation and Measurement of Conducted Emission in DC-DC convertor”, Conference Series, IOP Publishing - Journal of Physics: 1916 (2021) 012135, doi:10.1088/1742-6596/1916/1/012135.

[17]. https://www.csc.fi

[18]. https://www.comsol.co.in

[19]. https://www.rfglobalnet.com

[20]. Cadence OrCAD Solutions. [Online]. Available: http://www.cadence. com/products/orcad/pages/default.aspx

[21]. https://www.keysight.com

[22]. Ngspice. [Online]. Available: http://ngspice.sourceforge.net/

[23]. KiCad. [Online]. Available: http://www.kicad-pcb.org

[24]. H. Narayanan, Submodular functions and electrical networks. NorthHolland, 1997.

[25]. C. W. Ho, A. E. Ruehli, and P. A. Brennan, “The modified nodal approach to network analysis,” IEEE Transactions on Circuits and Systems, vol. 22, pp. 504–509, Jun 1975. [15] E. J. Mastascusa, Computer-Assisted Network and System Analysis. John Wiley and Sons, 1987

[26]. Wu, T. L., S. T. Chert, J. N. Huang, and Y. H. Lin, “Numerical and experimental investigation of radiation caused by the switching noise on the partitioned dc reference planes of high speed digital PCB,” IEEE Trans. Electromagn. Compat., Vol. 46, No. 1, 33–45, Feb. 2004.

[27]. Wu, T. L., H. H. Chuang, and T. K. Wang, “Overview of power integrity solutions on package and PCB: Decoupling and EBG isolation,” IEEE Trans. Electromagn. Compat., Vol. 52, No. 2, 346–356, May 2010.

[28]. Zhu, H.-R. and J.-F. Mao, “Localized planar EBG structure of CSRR for ultrawideband SSN mitigation and signal integrity improvement in mixed-signal systems,” IEEE Trans. Compon. Packag., Manuf. Technol., Vol. 3, No. 12, 2092–2100, Dec. 2013.

[29]. Yang, F.-R., K.-P. Ma, Y. Qian, and T. Itoh, “A uniplanar compact photonic-bandgap (UC-PBG) structure and its applications for microwave circuits,” IEEE Transactions on Microwave Theory and Techniques, Vol. 47, No. 8, 1509–1514, Aug. 1999

[30]. Li, L., B. Li, H.-H. Liu, and C.-H. Liang, “Locally resonant cavity cell model for electromagnetic bandgap structures,” IEEE Trans. Antennas Propag., Vol. 54, No. 1, 90–100, Jan. 2006.

[31]. L. Peng, C. L. Ruan, and J. Xiong. “Compact EBG for multi-band applications” IEEE Transactions on Antennas and Propagation, vol. 60, pp. 4440-4444, 2012.

[32]. X. L. Bao, G. Ruvio, and M. J. Ammann, “Low-profile dual-frequency GPS patch antenna enhanced with dual-band EBG structure,” Microw. Opt. Technol. Lett., vol. 49, no. 11, pp. 2630,-2634, Nov. 2007.

[33]. T. Kamgaing, and O. M. Ramahi, “Multiband Electromagnetic-Bandgap Structures for Applications in Small FormFactor Multichip Module Packages,” IEEE Trans. Microw. Theory Tech., vol. 56, no. 10, pp. 2293-2300, Oct. 2008.